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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,770	09/17/2003	Charles E. Moore	10030322-1	9421

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EXAMINER	
CHUNG, PHUNG M	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 07/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,770	MOORE ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13 and 16-19* is/are rejected.

7)☒ Claim(s) *14-15* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 U.S.C. § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

2. Claims 1-2, 4-8, 11-13 and 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright (5,264,740) in view of Eklow et al ("A Boundary-Scan Standard for Advanced Digital Networks" IEEE 1149.6, 2003, pgs. 76-83).

As per claims 1 and 7, Wright discloses a programmable voltage hysteresis on a voltale comparator, comprising:

A comparator (20) comprising a first input (22) to receive signal during board interconnect testing, and a second input (24) to receive a reference voltage; and

a programmable hysteresis circuit (26) coupled to at least one of the comparator inputs. (See Fig. 1, col. 1, lines 27-44 and col. 3, lines 34-64). Wright does not disclose boundary scan test receiver including a comparator to receive signals during board interconnect testing. However, Eklow et al disclose a boundary scan test receiver including a comparator to receive signals during board interconnect testing (Fig. 2, pg. 77, "IEEE 1149.6 physical interface to pg. 78, third paragraph). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the boundary scan test receiver including a comparator to receive signals as taught by Eklow et al into the comparator of Wright to include a boundary scan test receiver including a comparator to receive signals during board interconnect testing. The advantage of Eklow et al are: Reliable capture of decaying AC coupled waveforms; no degradation of mission performance; identification of all defects in the minimum defect model; operability with AC or DC coupling; and minimum impact to IEEE 1149.1 tools.

As per claim 2, Wright further discloses wherein the programmable hysteresis circuit comprises a programmable hysteresis voltage generator (col. 3, lines 49-64).

As per claim 4, Eklow et al further discloses that wherein the programmable hysteresis circuit comprises a programmable delay circuit (Fig. 2).

As per claims 5 and 6, Eklow et al further disclose a digital to analog converter driving a plurality of variable capacitances, the capacitances being coupled at various points along a chain of buffer elements and driving a chain of switchable delay elements (Figs. 2 and 3).

As per claim 8, Wright discloses a programmable voltage hystersis on a voltale comparator, comprising:

A plurality of comparators, each comparator (20) comprising a first input to receive signal during board interconnect testing, and a second input to receive a reference voltage and

a programmable hysteresis circuit (26) coupled to at least one of the comparator inputs. (See Fig. 1, col. 1, lines 10-44 and col. 3, lines 34-64). Wright does not disclose a boundary scan test receiver including comparator to receive signals during board interconnect testing. However, Eklow et al disclose a boundary scan test receiver including a comparator to receive signals during board interconnect testing (Fig. 2, pg. 77, "IEEE 1149.6 physical interface to pg. 78, third paragraph). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the boundary scan test receiver including a comparator to receive signals as taught by Eklow et al into the comparator of Wright to include a boundary scan test receiver including a comparator to receive signals during board interconnect testing. The advantage of Eklow et al are: Reliable capture of decaying AC coupled waveforms; no degradation of mission performance; identification of all defects in the minimum defect model; operability with AC or DC coupling; and minimum impact to IEEE 1149.1 tools.

As per claims 11-12 and 18-19, these method claims are rejected under similar rationale as set forth in the system claims 1 and 8.

As per claim 13, determining a noise level associated with signal paths of the board under test is inherent in the boundary scan test of Eklow et al.

As per claims 16 and 17, these method claims are rejected under similar rationale as set forth in the system claims 2 and 4.

3. Claims 3, 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wright (5,264,740) and Eklow et al ("A Boundary-Scan Standard for Advanced Digital Networks" IEEE 1149.6, 2003, pgs. 76-83) as applied to claims in view of Jenkins et al (5,610,545).

As per claim 3, the teaching of Wright and Eklow et al has been discussed above. They do not disclose wherein the programmable hysteresis voltage generator comprises a current digital-to-analog converter to sink current from one of the first and second inputs. However, Jenkins et al disclose the programmable hysteresis voltage generator comprises a current digital-to-analog converter to sink current from one of the first and second inputs (col. 3, lines 30-32 and lines 40-47). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the programmable hysteresis voltage generator comprises a current digital-to-analog converter to sink current from one of the first and second inputs as taught by Jenkins et al into the invention of Wright and Eklow et al to adjust the hysteresis differential to different preset and intermediate hysteresis levels.

As per claim 9, Jenkins et al further disclose: wherein the programmable hysteresis circuit comprises a programmable hysteresis voltage generator; the programmable hysteresis voltage generator comprises:

a) a voltage divider... (col. 1, lines 35-36);

b) a current digital-to-analog converter...(col. 3, lines 28-33); and

c) a current mirror... (col. 3, line 45).

As per claim 10, Jekins et al further disclose: wherein the programmable hysteresis circuit comprises a programmable hysteresis voltage generator; the programmable hysteresis voltage generator comprises:

a) a voltage divider... (col. 1, lines 35-36);

b) a current digital-to-analog converter...(col. 3, lines 28-33); and

c) a current mirror... (col. 3, line 45).

Allowable Subject Matter

4. Claims 14-15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. Applicant's arguments with respect to claims 1-19 have been considered but are moot in view of the new ground(s) of rejection.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571- 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Phung My Chung
Primary Patent Examiner